

10/829,527

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 001207.P004XC6	Application Number: Not yet assigned
	First Named Inventor: Benjamin S. Ting	
	Filing Date: Herewith	

U.S. PATENT DOCUMENTS						
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		Number Code ²	Kind (If known)			
<i>AT</i>		4,935,734		Austin	6/19/90	
<i>AT</i>		4,992,680		Benedetti, et al.	2/12/91	
<i>AT</i>		5,396,126		Britton, et al.	3/7/95	
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<i>AT</i>		PCT	9410754			5/11/94		
		PCT	9208286			5/14/92		
		EPO	0415542			3/6/91		
		UK	2180382			3/25/87		
		EPO	0630115A2			6/1/94		
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		PCT	9635261			11/7/96		
		PCT	9428475			12/8/94		
<i>AT</i>		UK	2295738			5/6/96		

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		4,720,780		Dolecek	1/19/88	
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		4,847,612		Kaplinsky	7/11/89	
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<i>19a</i>		5,469,003		Kean	11/21/95	
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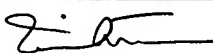
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✓		5,457,410		Ting	10/10/95	
		5,835,405		Tsui, et al.	11/10/98	
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		6,038,627		Plants	3/14/00	
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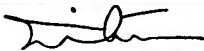
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		5,260,611		Cliff et al.	9/1993	
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OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
UT		Cliff, et al., "A Dual Granularity and Globally Interconnected Architecture for A Programmable Logic Device", 9/5/93, IEEE, pp. 7.3.1-7.3.5	
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		Minnick, R.C., "A Survey of Microcellular Research", vol. 14, no. 2, 4/1967, pp. 203-241.	
		SHOUP, R. G., "Programmable Cellular Logic Arrays," Abstract, Ph.D. Dissertation, Carnegie Mellon University, Pittsburgh, PA, March 1970, (partial) pp. ii-121.	
		SPANDORFER, L.M., "Synthesis of Logic Functions on an Array of Integrated Circuits," Contract No. AF 19 (628) 2907, Project No. 4645, Task No. 464504, Final Report, November 30, 1965.	
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		ATMEL Field Programmable Arrays, AT 6000 Series, 1993, p. 1-16. No month	
		Motorola Project Brief, "MPA10xx Field Programmable Gate Arrays," September 27, 1993, 4 pages.	
UT		Altera Corporation Data Sheet, Flex EPF81188 12,000 Gate Programmable Logic Device, September 1992, Ver. 1, pp. 1-20.	

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		DEVADES, S., et al., "Boolean Decomposition of Programmable Logic Arrays," IEEE 1988, pp. 2.5.1 - 2.5.5. <i>No month</i>	
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		LIU, D.L., et al., "Design of Large Embedded CMOS PLA's for Built-In Self-test," IEEE Transactions on Computed-Aided Design, Vol. 7, No. 1, January 1988, pp. 50-53.	
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